# 3A, 28V INPUT, STEP DOWN SWIFT™ DC/DC CONVERTER WITH ECO-MODE™

## FEATURES

- **3.5V to 28V Input Voltage Range**
- **Adjustable Output Voltage Down to 0.8V**
- **Integrated 80 mΩ High Side MOSFET Supports up to 3A Continuous Output Current**
- **High Efficiency at Light Loads with a Pulse Skipping Eco-mode™**
- **Fixed 570kHz Switching Frequency**
- **Typical 1μA Shutdown Quiescent Current**
- **Adjustable Slow Start Limits Inrush Currents**
- **Programmable UVLO Threshold**
- **Overvoltage Transient Protection**
- **Cycle by Cycle Current Limit, Frequency Fold Back and Thermal Shutdown Protection**
- **Available in Easy-to-Use SOIC8 Package**
- **Supported by SwitcherPro™ Software Tool (http://focus.ti.com/docs/toolsw/folders/print/switcherpro.html)**
- **For SWIFT™ Documentation, See the TI Website at www.ti.com/swift**

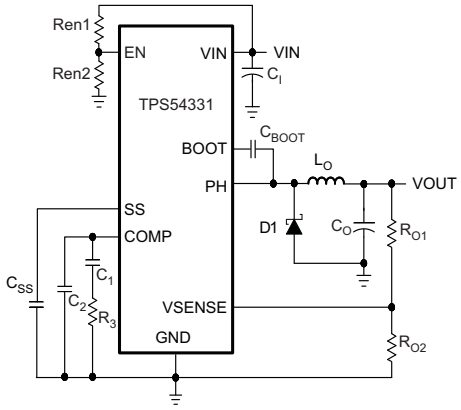
## APPLICATIONS

- **Consumer Applications such as Set-Top Boxes, CPE Equipment, LCD Displays, Peripherals, and Battery Chargers**
- **Industrial and Car Audio Power Supplies**
- **5V, 12V and 24V Distributed Power Systems**

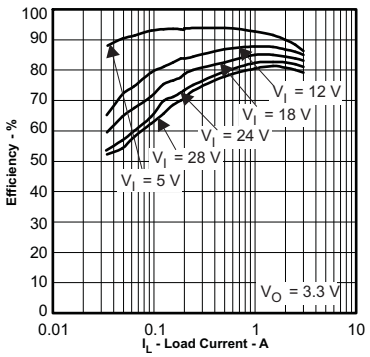
## DESCRIPTION

The TPS54331 is a 28-V, 3-A non-synchronous buck converter that integrates a low Rds(on) high side MOSFET. To increase efficiency at light loads, a pulse skipping Eco-mode™ feature is automatically activated. Furthermore, the 1 μA shutdown supply current allows the device to be used in battery powered applications. Current mode control with internal slope compensation simplifies the external compensation calculations and reduces component count while allowing the use of ceramic output capacitors. A resistor divider programs the hysteresis of the input under-voltage lockout. An overvoltage transient protection circuit limits voltage overshoots during startup and transient conditions. A cycle by cycle current limit scheme, frequency fold back and thermal shutdown protect the device and the load in the event of an overload condition. The TPS54331 is available in an 8-pin SOIC package that has been internally optimized to improve thermal performance.

**SIMPLIFIED SCHEMATIC**




**EFFICIENCY**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION(1)

| $T_J$ | PACKAGE | SWITCHING FREQUENCY | PART NUMBER(2) |
|---|---|---|---|
| –40°C to 150°C | 8 pin SOIC | 570 kHz | TPS54331D |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) The D package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54331DR). See applications section of data sheet for layout information.

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | VALUE | UNIT |
|---|---|---|---|
| Input Voltage | VIN | –0.3 to 30 | V |
| | EN | –0.3 to 5 | |
| | BOOT | 38 | |
| | VSENSE | –0.3 to 3 | |
| | COMP | –0.3 to 3 | |
| | SS | –0.3 to 3 | |
| Output Voltage | BOOT-PH | 8 | V |
| | PH | –0.6 to 30 | |
| | PH (10 ns transient from ground to negative peak) | –5 | |
| Source Current | EN | 100 | µA |
| | BOOT | 100 | mA |
| | VSENSE | 10 | µA |
| | PH | 9 | A |
| Sink Current | VIN | 9 | A |
| | COMP | 100 | µA |
| | SS | 200 | |
| Electrostatic Discharge (HBM) | | 2 | kV |
| Electrostatic Discharge (CDM) | | 500 | V |
| Operating Junction Temperature | | –40 to 150 | °C |
| Storage Temperature | | –65 to 150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## PACKAGE DISSIPATION RATINGS(1) (2)(3)

| PACKAGE | THERMAL IMPEDANCE JUNCTION TO AMBIENT | PSEUDO THERMAL IMPEDANCE JUNCTION TO TOP |
|---|---|---|
| SOIC8 | 100 °C/W | 5 °C/W |

(1) Maximum power dissipation may be limited by overcurrent protection
(2) Power rating at a specific ambient temperature $T_A$ should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. Thermal management of the PCB should strive to keep the junction temperature at or below 150°C for best performance and long-term reliability. See *power dissipation estimate* in application section of this data sheet for more information.
(3) Test board conditions:
a. 2 inches x 1.5 inches, 2 layers, thickness: 0.062 inch
b. 2-ounce copper traces located on the top and bottom of the PCB
c. 6 thermal vias located under the device package

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Operating Input Voltage on (VIN pin) | 3.5 | | 28 | V |
| Operating junction temperature, $T_J$ | –40 | | 150 | °C |

## ELECTRICAL CHARACTERISTICS

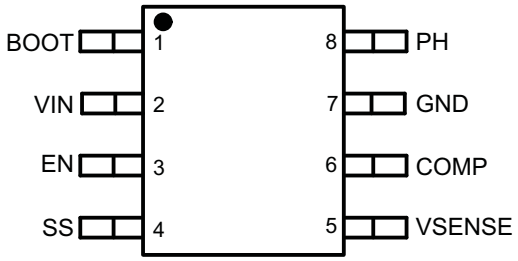
$T_J$ = –40°C to 150°C, VIN = 3.5V to 28V (unless otherwise noted)

| DESCRIPTION | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **SUPPLY VOLTAGE (VIN PIN)** | | | | | |
| Internal undervoltage lockout threshold | Rising and Falling | | | 3.5 | V |
| Shutdown supply current | EN = 0V, VIN = 12V, –40°C to 85°C | | 1 | 4 | µA |
| Operating – non switching supply current | VSENSE = 0.85 V | | 110 | 190 | µA |
| **ENABLE AND UVLO (EN PIN)** | | | | | |
| Enable threshold | Rising and Falling | | 1.25 | 1.35 | V |
| Input current | Enable threshold – 50 mV | | -1 | | µA |
| Input current | Enable threshold + 50 mV | | -4 | | µA |
| **VOLTAGE REFERENCE** | | | | | |
| Voltage reference | | 0.772 | 0.8 | 0.828 | V |
| **HIGH-SIDE MOSFET** | | | | | |
| On resistance | BOOT-PH = 3 V, VIN = 3.5 V | | 115 | 200 | mΩ |
| | BOOT-PH = 6 V, VIN = 12 V | | 80 | 150 | |
| **ERROR AMPLIFIER** | | | | | |
| Error amplifier transconductance (gm) | –2 µA < ICOMP < 2 µA, V(COMP) = 1 V | | 92 | | µmhos |
| Error amplifier DC gain(1) | VSENSE = 0.8 V | | 800 | | V/V |
| Error amplifier unity gain bandwidth(1) | 5 pF capacitance from COMP to GND pins | | 2.7 | | MHz |
| Error amplifier source/sink current | V(COMP) = 1.0 V, 100 mV overdrive | | ±7 | | µA |
| Switch current to COMP transconductance | VIN = 12 V | | 12 | | A/V |
| **SWITCHING FREQUENCY** | | | | | |
| TPS54331 Switching Frequency | VIN = 12V, 25°C | 456 | 570 | 684 | kHz |
| Minimum controllable on time | VIN = 12V, 25°C | | 105 | 130 | ns |
| Maximum controllable duty ratio(1) | BOOT-PH = 6 V | 90 | 93 | | % |
| **PULSE SKIPPING ECO-MODE™** | | | | | |
| Pulse skipping Eco-mode™ switch current threshold | | | 160 | | mA |
| **CURRENT LIMIT** | | | | | |
| Current limit threshold | VIN = 12 V | 3.5 | 5.8 | | A |
| **THERMAL SHUTDOWN** | | | | | |
| Thermal Shutdown | | | 165 | | °C |
| **SLOW START (SS PIN)** | | | | | |
| Charge current | V(SS) = 0.4 V | | 2 | | µA |
| SS to VSENSE matching | V(SS) = 0.4 V | | 10 | | mV |

(1) Specified by design

# DEVICE INFORMATION

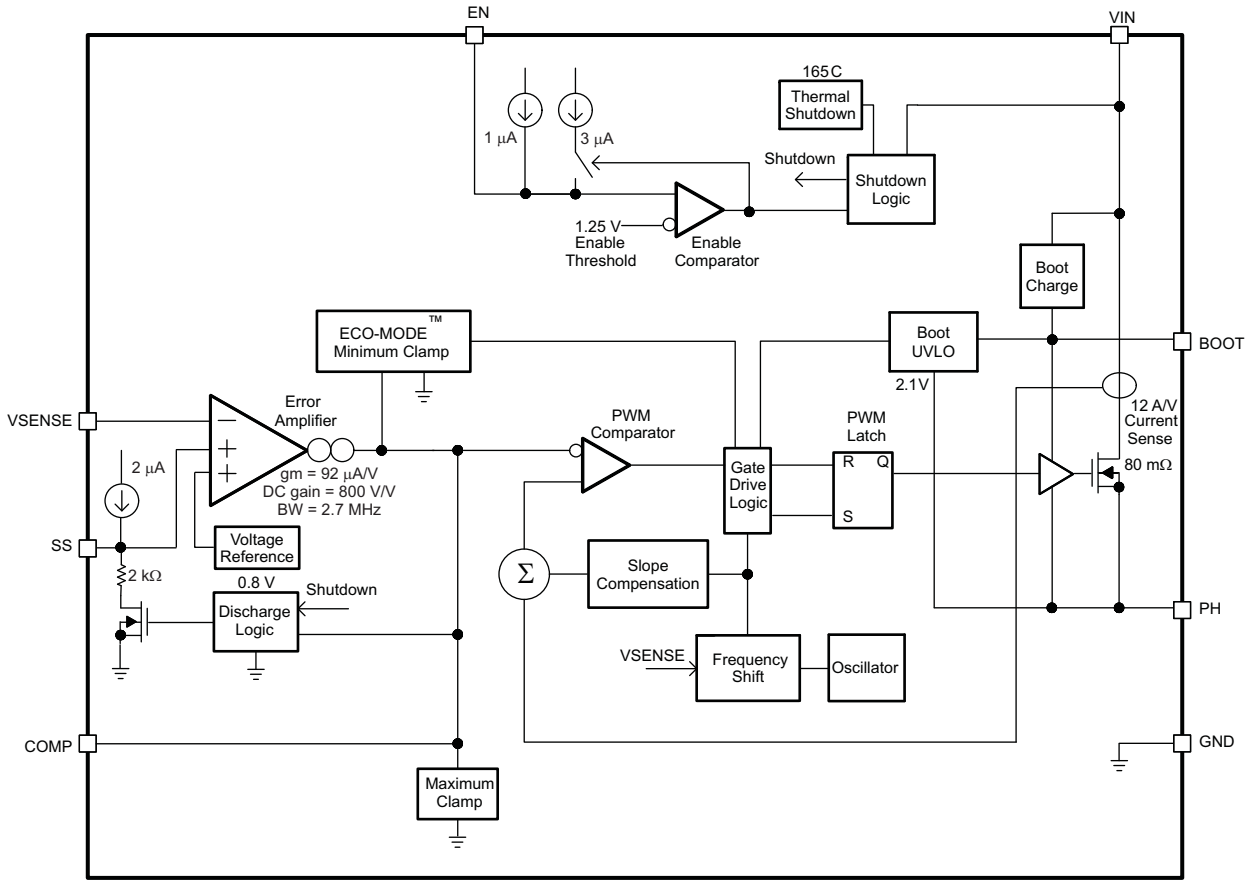
## PIN ASSIGNMENTS




### TERMINAL FUNCTIONS

| TERMINAL | | DESCRIPTION |
|---|---|---|
| NAME | NO. | |
| BOOT | 1 | A 0.1 µF bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor falls below the minimum requirement, the high-side MOSFET is forced to switch off until the capacitor is refreshed. |
| VIN | 2 | Input supply voltage, 3.5 V to 28 V. |
| EN | 3 | Enable pin. Pull below 1.25V to disable. Float to enable. Programming the input undervoltage lockout with two resistors is recommended. |
| SS | 4 | Slow start pin. An external capacitor connected to this pin sets the output rise time. |
| VSENSE | 5 | Inverting node of the gm error amplifier. |
| COMP | 6 | Error amplifier output, and input to the PWM comparator. Connect frequency compensation components to this pin. |
| GND | 7 | Ground. |
| PH | 8 | The source of the internal high-side power MOSFET. |

## FUNCTIONAL BLOCK DIAGRAM




## TYPICAL CHARACTERISTICS

## CHARACTERIZATION CURVES

**ON RESISTANCE VS JUNCTION TEMPERATURE**

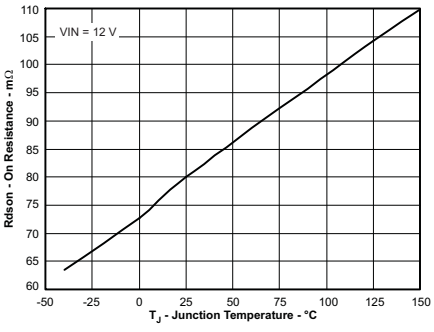



**Figure 1.**

**SHUTDOWN QUIESCENT CURRENT VS INPUT VOLTAGE**

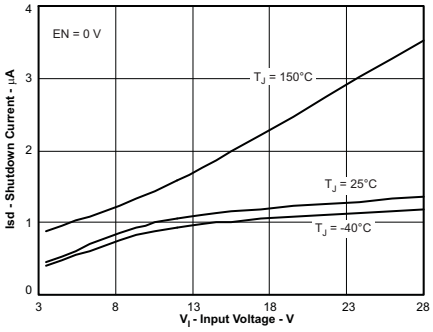



**Figure 2.**

**SWITCHING FREQUENCY VS JUNCTION TEMPERATURE**

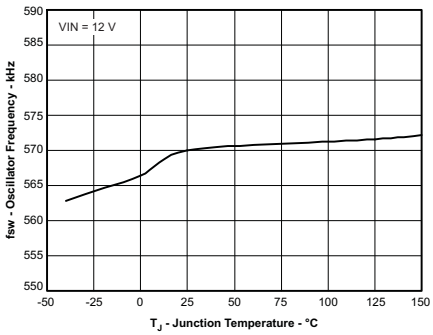



**Figure 3.**

## TYPICAL CHARACTERISTICS (continued)

**VOLTAGE REFERENCE VS JUNCTION TEMPERATURE**

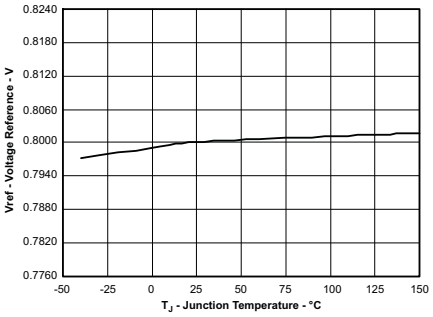



Figure 4.

**MINIMUM CONTROLLABLE ON TIME VS JUNCTION TEMPERATURE**

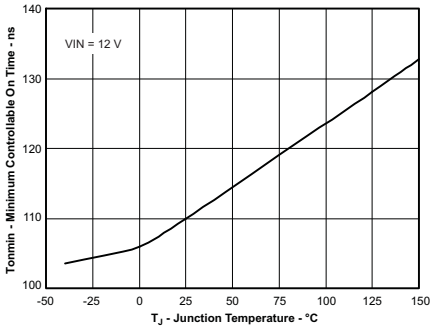



Figure 5.

**MINIMUM CONTROLLABLE DUTY RATIO VS JUNCTION TEMPERATURE**

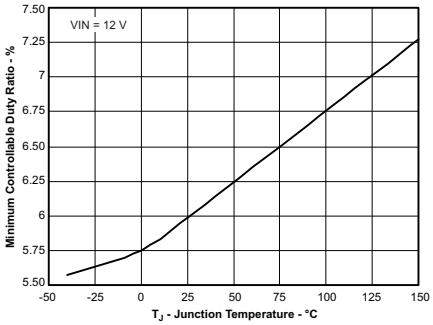



Figure 6.

**SS CHARGE CURRENT VS JUNCTION TEMPERATURE**

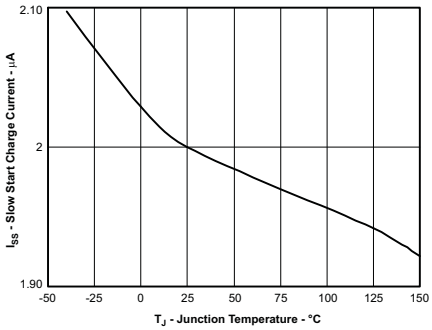



Figure 7.

**CURRENT LIMIT THRESHOLD VS INPUT VOLTAGE**

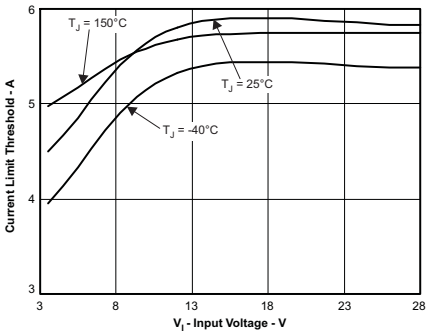



Figure 8.

## SUPPLEMENTAL APPLICATION CURVES

**TYPICAL MINIMUM OUTPUT VOLTAGE VS INPUT VOLTAGE**

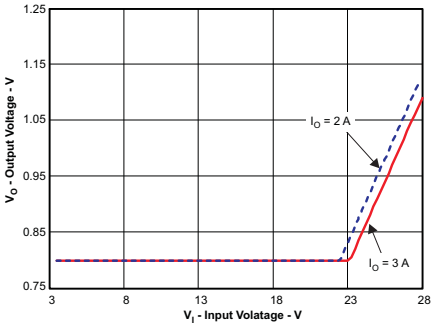



Figure 9.

**TYPICAL MAXIMUM OUTPUT VOLTAGE VS INPUT VOLTAGE**

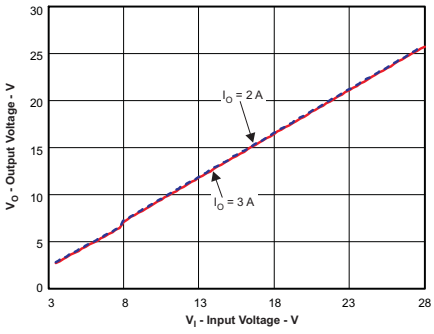



Figure 10.

**MAXIMUM POWER DISSIPATION VS JUNCTION TEMPERATURE**

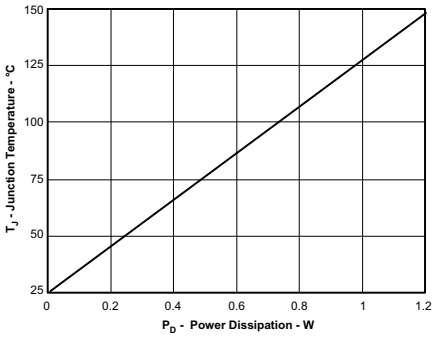



Figure 11.

## TYPICAL CHARACTERISTICS (continued)

## OVERVIEW

The TPS54331 is a 28-V, 3-A, step-down (buck) converter with an integrated high-side n-channel MOSFET. To improve performance during line and load transients, the device implements a constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design. The TPS54331 has a pre-set switching frequency of 570kHz.

The TPS54331 needs a minimum input voltage of 3.5V to operate normally. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under-voltage lockout (UVLO) with two external resistors. In addition, the pull-up current provides a default condition when the EN pin is floating for the device to operate. The operating current is 110 μA typically when not switching and under no load. When the device is disabled, the supply current is 1μA typically.

The integrated 80 mΩ high-side MOSFET allows for high efficiency power supply designs with continuous output currents up to 3A.

The TPS54331 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high-side MOSFET off when the voltage falls below a preset threshold of 2.1V typically. The output voltage can be stepped down to as low as the reference voltage.

By adding an external capacitor, the slow start time of the TPS54331 can be adjustable which enables flexible output filter selection.

To improve the efficiency at light load conditions, the TPS54331 enters a special pulse skipping Eco-mode™ when the peak inductor current drops below 160mA typically.

The frequency foldback reduces the switching frequency during startup and over current conditions to help control the inductor current. The thermal shut down gives the additional protection under fault conditions.

## DETAILED DESCRIPTION

### FIXED FREQUENCY PWM CONTROL

The TPS54331 uses a fixed frequency, peak current mode control. The internal switching frequency of the TPS54331 is fixed at 570kHz.

### ECO-MODE™

The TPS54331 is designed to operate in pulse skipping Eco-mode™ at light load currents to boost light load efficiency. When the peak inductor current is lower than 160 mA typically, the COMP pin voltage falls to 0.5V typically and the device enters Eco-mode™ . When the device is in Eco-mode™, the COMP pin voltage is clamped at 0.5V internally which prevents the high side integrated MOSFET from switching. The peak inductor current must rise above 160mA for the COMP pin voltage to rise above 0.5V and exit Eco-mode™. Since the integrated current comparator catches the peak inductor current only, the average load current entering Eco-mode™ varies with the applications and external output filters.

### VOLTAGE REFERENCE (Vref)

The voltage reference system produces a ±2% initial accuracy voltage reference (±3.5% over temperature) by scaling the output of a temperature stable bandgap circuit. The typical voltage reference is designed at 0.8V.

### BOOTSTRAP VOLTAGE (BOOT)

The TPS54331 has an integrated boot regulator and requires a 0.1μF ceramic capacitor between the BOOT and PH pin to provide the gate drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the TPS54331 is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than 2.1V typically.

## ENABLE AND ADJUSTABLE INPUT UNDER-VOLTAGE LOCKOUT (VIN UVLO)

The EN pin has an internal pull-up current source that provides the default condition of the TPS54331 operating when the EN pin floats.

The TPS54331 is disabled when the VIN pin voltage falls below internal VIN UVLO threshold. It is recommended to use an external VIN UVLO to add Hysteresis unless VIN is greater than (VOUT + 2V). To adjust the VIN UVLO with Hysteresis, use the external circuitry connected to the EN pin as shown in Figure 12. Once the EN pin voltage exceeds 1.25V, an additional 3µA of hysteresis is added. Use Equation 1 and Equation 2 to calculate the resistor values needed for the desired VIN UVLO threshold voltages. The $V_{START}$ is the input start threshold voltage, the $V_{STOP}$ is the input stop threshold voltage and the $V_{EN}$ is the enable threshold voltage of 1.25V. The $V_{STOP}$ should always be greater than 3.5V.

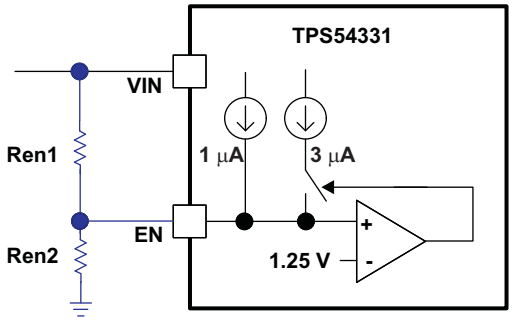



**Figure 12. Adjustable Input Under-Voltage Lockout**

$$Ren1 = \frac{V_{START} - V_{STOP}}{3\ \mu A} \quad (1)$$

$$Ren2 = \frac{V_{EN}}{\frac{V_{START} - V_{EN}}{Ren1} + 1\ \mu A} \quad (2)$$

## PROGRAMMABLE SLOW START USING SS PIN

It is highly recommended to program the slow start time externally because no slow start time is implemented internally. The TPS54331 effectively uses the lower voltage of the internal voltage reference or the SS pin voltage as the power supply's reference voltage fed into the error amplifier and will regulate the output accordingly. A capacitor (Css) on the SS pin to ground implements a slow start time. The TPS54331 has an internal pull-up current source of 2µA that charges the external slow start capacitor. The equation for the slow start time (10% to 90%) is shown in Equation 3 . The Vref is 0.8V and the Iss current is 2µA.

$$T_{SS}(ms) = \frac{C_{SS}(nF) \times V_{ref}(V)}{I_{SS}(\mu A)} \quad (3)$$

The slow start time should be set between 1ms to 10ms to ensure good start-up behavior. The slow start capacitor should be no more than 27nF.

If during normal operation, the input voltage drops below the VIN UVLO threshold, or the EN pin is pulled below 1.25V, or a thermal shutdown event occurs, the TPS54331 stops switching.

## ERROR AMPLIFIER

The TPS54331 has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the internal effective voltage reference presented at the input of the error amplifier. The transconductance of the error amplifier is 92 µA/V during normal operation. Frequency compensation components are connected between the COMP pin and ground.

## SLOPE COMPENSATION

In order to prevent the sub-harmonic oscillations when operating the device at duty cycles greater than 50%, the TPS54331 adds a built-in slope compensation which is a compensating ramp to the switch current signal.

## CURRENT MODE COMPENSATION DESIGN

To simplify design efforts using the TPS54331, the typical designs for common applications are listed in Table 1. For designs using ceramic output capacitors, proper derating of ceramic output capacitance is recommended when doing the stability analysis. This is because the actual ceramic capacitance drops considerably from the nominal value when the applied voltage increases. Advanced users may refer to the *Step by Step Design Procedure* in the Application Information section for the detailed guidelines or use SwitcherPro™ Software tool (http://focus.ti.com/docs/toolsw/folders/print/switcherpro.html).

**Table 1. Typical Designs (Referring to Simplified Schematic on page 1)**

| VIN (V) | VOUT (V) | $F_{sw}$ (kHz) | $L_o$ (µH) | $C_o$ | $R_{O1}$ (kΩ) | $R_{O2}$ (kΩ) | $C_2$ (pF) | $C_1$ (pF) | $R_3$ (kΩ) |
|---|---|---|---|---|---|---|---|---|---|
| 12 | 5 | 570 | 6.8 | Ceramic 33 µFx2 | 10 | 1.91 | 39 | 4700 | 49.9 |
| 12 | 3.3 | 570 | 6.8 | Ceramic 47µFx2 | 10 | 3.24 | 47 | 1000 | 29.4 |
| 12 | 1.8 | 570 | 4.7 | Ceramic 100 µF | 10 | 8.06 | 68 | 5600 | 29.4 |
| 12 | 0.9 | 570 | 3.3 | Ceramic 100 µFx2 | 10 | 80.6 | 56 | 5600 | 29.4 |
| 12 | 5 | 570 | 6.8 | Aluminum 330 µF/160 mΩ | 10 | 1.91 | 68 | 120 | 29.4 |
| 12 | 3.3 | 570 | 6.8 | Aluminum 470 µF/160 mΩ | 10 | 3.24 | 82 | 220 | 10 |
| 12 | 1.8 | 570 | 4.7 | SP 100 µF/15 mΩ | 10 | 8.06 | 68 | 5600 | 29.4 |
| 12 | 0.9 | 570 | 3.3 | SP 330 µF/12 mΩ | 10 | 80.6 | 100 | 1200 | 49.9 |

## OVERCURRENT PROTECTION AND FREQUENCY SHIFT

The TPS54331 implements current mode control that uses the COMP pin voltage to turn off the high-side MOSFET on a cycle by cycle basis. Every cycle the switch current and the COMP pin voltage are compared; when the peak inductor current intersects the COMP pin voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, causing the switch current to increase. The COMP pin has a maximum clamp internally, which limit the output current.

The TPS54331 provides robust protection during short circuits. There is potential for overcurrent runaway in the output inductor during a short circuit at the output. The TPS54331 solves this issue by increasing the off time during short circuit conditions by lowering the switching frequency. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0V to 0.8V on VSENSE pin. The relationship between the switching frequency and the VSENSE pin voltage is shown in Table 2.

**Table 2. Switching Frequency Conditions**

| SWITCHING FREQUENCY | VSENSE PIN VOLTAGE |
|---|---|
| 570 kHz | VSENSE ≥ 0.6 V |
| 570 kHz / 2 | 0.6 V > VSENSE ≥ 0.4 V |
| 570 kHz / 4 | 0.4 V > VSENSE ≥ 0.2 V |
| 570 kHz / 8 | 0.2 V > VSENSE |

## OVERVOLTAGE TRANSIENT PROTECTION

The TPS54331 incorporates an overvoltage transient protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and internal thresholds. When the VSENSE pin voltage goes above 109% × Vref, the high-side MOSFET will be forced off. When the VSENSE pin voltage falls below 107% × Vref, the high-side MOSFET will be enabled again.

## THERMAL SHUTDOWN

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 165°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 165°C, the device reinitiates the power up sequence.

## APPLICATION INFORMATION

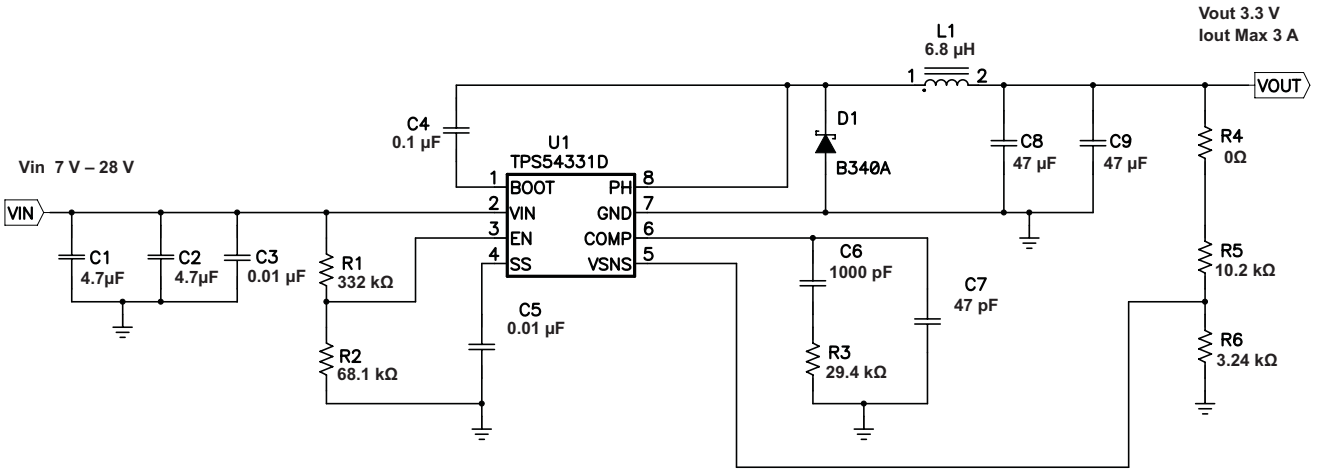



**Figure 13. Typical Application Schematic**

## STEP BY STEP DESIGN PROCEDURE

The following design procedure can be used to select component values for the TPS54331. Alternately, the SwitcherPro™Software may be used to generate a complete design. The SwitcherPro™ Software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Input voltage range
- Output voltage
- Input ripple voltage
- Output ripple voltage
- Output current rating
- Operating frequency

For this design example, use the following as the input parameters

**Table 3. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage range | 7 V to 28V |
| Output voltage | 3.3 V |
| Input ripple voltage | 300 mV |
| Output ripple voltage | 30 mV |
| Output current rating | 3 A |
| Operating Frequency | 570 kHz |

## SWITCHING FREQUENCY

The switching frequency for the TPS54331 is fixed at 570 kHz.

## OUTPUT VOLTAGE SET POINT

The output voltage of the TPS54331 is externally adjustable using a resistor divider network. In the application circuit of Figure 13, this divider network is comprised of R5 and R6. The relationship of the output voltage to the resistor divider is given by Equation 4 and Equation 5:

$$R6 = \frac{R5 \times V_{REF}}{V_{OUT} - V_{REF}} \quad (4)$$

$$V_{OUT} = V_{REF} \times \left[\frac{R5}{R6} + 1\right] \quad (5)$$

Choose R5 to be approximately 10.0 kΩ. Slightly increasing or decreasing R5 can result in closer output voltage matching when using standard value resistors. In this design, R4 = 10.2 kΩ and R = 3.24 kΩ, resulting in a 3.31 V output voltage. The zero ohm resistor R4 is provided as a convenient place to break the control loop for stability testing.

## INPUT CAPACITORS

The TPS54331 requires an input decoupling capacitor and depending on the application, a bulk input capacitor. The typical recommended value for the decoupling capacitor is 10 µF. A high-quality ceramic type X5R or X7R is recommended. The voltage rating should be greater than the maximum input voltage. A smaller value may be used as long as all other requirements are met; however 10 µF has been shown to work well in a wide variety of circuits. Additionally, some bulk capacitance may be needed, especially if the TPS54331 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but should be rated to handle the maximum input voltage including ripple voltage, and should filter the output so that input ripple voltage is acceptable. For this design two 4.7 µF capacitors are used for the input decoupling capacitor. They are X7R dielectric rated for 50 V. The equivalent series resistance (ESR) is approximately 2mΩ, and the current rating is 3 A. Additionally, a small 0.01 µF capacitor is included for high frequency filtering.

This input ripple voltage can be approximated by Equation 6

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{SW}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \quad (6)$$

Where $I_{OUT(MAX)}$ is the maximum load current, $f_{SW}$ is the switching frequency, $C_{BULK}$ is the bulk capacitor value and $ESR_{MAX}$ is the maximum series resistance of the bulk capacitor.

The maximum RMS ripple current also needs to be checked. For worst case conditions, this can be approximated by Equation 7

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \quad (7)$$

In this case, the input ripple voltage would be 143 mV and the RMS ripple current would be 1.5 A. It is also important to note that the actual input voltage ripple will be greatly affected by parasitics associated with the layout and the output impedance of the voltage source. The actual input voltage ripple for this circuit is shown in Design Parameters and is larger than the calculated value. This measured value is still below the specified input limit of 300 mV. The maximum voltage across the input capacitors would be VIN max plus ΔVIN/2. The chosen bulk and bypass capacitors are each rated for 50 V and the ripple current capacity is greater than 3 A, both providing ample margin. It is very important that the maximum ratings for voltage and current are not exceeded under any circumstance.

## OUTPUT FILTER COMPONENTS

Two components need to be selected for the output filter, L1 and C2. Since the TPS54331 is an externally compensated device, a wide range of filter component types and values can be supported.

### Inductor Selection

To calculate the minimum value of the output inductor, use Equation 8

$$L_{MIN} = \frac{V_{OUT(MAX)} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{SW}} \quad (8)$$

$K_{IND}$ is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. In general, this value is at the discretion of the designer; however, the following guidelines may be used. For designs using low ESR output capacitors such as ceramics, a value as high as $K_{IND}$ = 0.3 may be used. When using higher ESR output capacitors, $K_{IND}$ = 0.2 yields better results.

For this design example, use $K_{IND}$ = 0.3 and the minimum inductor value is calculated to be 5.7µH. For this design, a large value was chosen: 6.8 µH.

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be found from Equation 9

$$I_{L(RMS)} = \sqrt{I^2_{OUT(MAX)} + \frac{1}{12} \times \left( \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8} \right)^2} \quad (9)$$

and the peak inductor current can be determined with Equation 10

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}} \quad (10)$$

For this design, the RMS inductor current is 3.01 A and the peak inductor current is 3.47 A. The chosen inductor is a Sumida CDRH103-6R8 6.8 µH. It has a saturation current rating of 3.84 A and an RMS current rating of 3.60 A, meeting these requirements. Smaller or larger inductor values can be used depending on the amount of ripple current the designer wishes to allow so long as the other design requirements are met. Larger value inductors will have lower ac current and result in lower output voltage ripple, while smaller inductor values will increase ac current and output voltage ripple. In general, inductor values for use with the TPS54331 are in the range of 6.8 µH to 47µH.

### Capacitor Selection

The important design factors for the output capacitor are dc voltage rating, ripple current rating, and equivalent series resistance (ESR). The dc voltage and ripple current ratings cannot be exceeded. The ESR is important because along with the inductor current it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed loop crossover frequency of the design and LC corner frequency of the output filter. In general, it is desirable to keep the closed loop crossover frequency at less than 1/5 of the switching frequency. With high switching frequencies such as the 570-kHz frequency of this design, internal circuit limitations of the TPS54331 limit the practical maximum crossover frequency to about 25 kHz. In general, the closed loop crossover frequency should be higher than the corner frequency determined by the load impedance and the output capacitor. This limits the minimum capacitor value for the output filter to:

$$C_{O\_min} = 1/(2 \times \pi \times R_O \times F_{CO\_max}) \quad (11)$$

Where $R_O$ is the output load impedance ($V_O/I_O$) and $f_{CO}$ is the desired crossover frequency. For a desired maximum crossover of 25 kHz the minimum value for the output capacitor is around 5.8µF. This may not satisfy the output ripple voltage requirement. The output ripple voltage consists of two components; the voltage change due to the charge and discharge of the output filter capacitance and the voltage change due to the ripple current times the ESR of the output filter capacitor. The output ripple voltage can be estimated by:

$$V_{OPP} = I_{LPP}\left[\frac{(D - 0.5)}{4 \times F_{SW} \times C_O} + R_{ESR}\right] \quad (12)$$

Where $N_C$ is the number of output capacitors in parallel.

The maximum ESR of the output capacitor can be determined from the amount of allowable output ripple as specified in the initial design parameters. The contribution to the output ripple voltage due to ESR is the inductor ripple current times the ESR of the output filter, so the maximum specified ESR as listed in the capacitor data sheet is given by Equation 13

$$ESR_{max} = \frac{V_{OPPMAX}}{I_{LPP}} - \frac{(D - 0.5)}{4 \times F_{SW} \times C_O} \quad (13)$$

Where $V_{OPPMAX}$ is the desired maximum peak-to-peak output ripple. The maximum RMS ripple current in the output capacitor is given by Equation 14.

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left( \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times N_C} \right) \quad (14)$$

For this design example, two 47-µF ceramic output capacitors are chosen for C8 and C9. These are TDK C3216X5R0J476MT, rated at 6.3 V with a maximum ESR of 2 mΩ and a ripple current rating in excess of 3 A. The calculated total RMS ripple current is 161 mA ( 80.6 mA each) and the maximum total ESR required is 43 mΩ. These output capacitors exceed the requirements by a wide margin and will result in a reliable, high-performance design. it is important to note that the actual capacitance in circuit may be less than the catalog value when the output is operating at the desired output of 3.3 V The selected output capacitor must be rated for a voltage greater than the desired output voltage plus ½ the ripple voltage. Any derating amount must also be included. Other capacitor types work well with the TPS54331, depending on the needs of the application.

## COMPENSATION COMPONENTS

The external compensation used with the TPS54331 allows for a wide range of output filter configurations. A large range of capacitor values and types of dielectric are supported. The design example uses ceramic X5R dielectric output capacitors, but other types are supported.

A Type II compensation scheme is recommended for the TPS54331. The compensation components are chosen to set the desired closed loop cross over frequency and phase margin for output filter components. The type II compensation has the following characteristics; a dc gain component, a low frequency pole, and a mid frequency zero / pole pair.

The dc gain is determined by Equation 15:

$$G_{DC} = \frac{V_{ggm} \times V_{REF}}{V_O} \quad (15)$$

Where:

$V_{ggm}$ = 800
$V_{REF}$ = 0.8 V

The low-frequency pole is determined by Equation 16:

$$V_{PO} = 1/(2 \times \pi \times R_{OO} \times C_Z) \quad (16)$$

The mid-frequency zero is determined by Equation 17:

$$F_{Z1} = 1/(2 \times \pi \times R_Z \times C_Z) \quad (17)$$

And, the mid-frequency pole is given by Equation 18:

$$F_{P1} = 1/(2 \times \pi \times R_Z \times C_P) \quad (18)$$

The first step is to choose the closed loop crossover frequency. In general, the closed-loop crossover frequency should be less than 1/8 of the minimum operating frequency, but for the TPS54331it is recommended that the maximum closed loop crossover frequency be not greater than 25 kHz. Next, the required gain and phase boost of the crossover network needs to be calculated. By definition, the gain of the compensation network must be the inverse of the gain of the modulator and output filter. For this design example, where the ESR zero is much higher than the closed loop crossover frequency, the gain of the modulator and output filter can be approximated by Equation 19:

$$\text{Gain} = -20\log\left(2 \times \pi \times R_{SENSE} \times F_{CO} \times C_O\right) \quad (19)$$

Where:

$R_{SENSE}$ = 1Ω/12
$F_{CO}$ = Closed-loop crossover frequency
$C_O$ = Output capacitance

The phase loss is given by Equation 20:

$$PL = a\tan\left(2 \times \pi \times F_{CO} \times R_{ESR} \times C_O\right) - a\tan\left(2 \times \pi \times F_{CO} \times R_O \times C_O\right) \quad (20)$$

Where:

$R_{ESR}$ = Equivalent series resistance of the output capacitor
$R_O = V_O/I_O$

The measured overall loop response for the circuit is given in Figure 20. Note that the actual closed loop crossover frequency is higher than intended at about 25 kHz. This is primarily due to variation in the actual values of the output filter components and tolerance variation of the internal feed-forward gain circuitry. Overall the design has greater than 60 degrees of phase margin and will be completely stable over all combinations of line and load variability.

Now that the phase loss is known the required amount of phase boost to meet the phase margin requirement can be determined. The required phase boost is given by Equation 21:

$$PB = \left(PM - 90\,\text{deg}\right) - PL \quad (21)$$

Where PM = the desired phase margin.

A zero / pole pair of the compensation network will be placed symmetrically around the intended closed loop frequency to provide maximum phase boost at the crossover point. The amount of separation can be determined by Equation 22 and the resultant zero and pole frequencies are given by Equation 23 and Equation 24

$$k = \tan\left(\frac{PB}{2} + 45\,\text{deg}\right) \quad (22)$$

$$F_{Z1} = \frac{F_{CO}}{k} \quad (23)$$

$$F_{P1} = F_{CO} \times k \quad (24)$$

The low-frequency pole is set so that the gain at the crossover frequency is equal to the inverse of the gain of the modulator and output filter. Due to the relationships established by the pole and zero relationships, the value of $R_Z$ can be derived directly by Equation 25 :

$$R_Z = \frac{2 \times \pi \times F_{CO} \times V_O \times C_O \times R_{OA}}{GM_{ICOMP} \times V_{ggm} \times V_{REF}} \quad (25)$$

Where:

$V_O$ = Output voltage
$C_O$ = Output capacitance
$F_{CO}$ = Desired crossover frequency
$R_{OA}$ = 8 MΩ
$GM_{COMP}$ = 12 A/V
$V_{ggm}$ = 800
$V_{REF}$ = 0.8 V

With $R_Z$ known, $C_Z$ and $C_P$ can be calculated using Equation 26 and Equation 27:

$$C_Z = \frac{1}{2 \times \pi \times F_{Z1} \times R_z} \quad (26)$$

$$C_P = \frac{1}{2 \times \pi \times F_{P1} \times R_z} \quad (27)$$

For this design, the two 47-µF output capacitors are used. For ceramic capacitors, the actual output capacitance is less than the rated value when the capacitors have a dc bias voltage applied. This is the case in a dc/dc converter. The actual output capacitance may be as low as 54 µF. The combined ESR is approximately .001 Ω.

Using Equation 19 and Equation 20, the output stage gain and phase loss are equivalent as:

Gain = –2.26 dB

and

PL - –83.52 degrees

For 70 degrees of phase margin, Equation 21 requires 63.52 degrees of phase boost.

Equation 22, Equation 23, and Equation 24 are used to find the zero and pole frequencies of:

$F_{Z1}$ = 5883 Hz

And

$F_{P1}$ = 106200 Hz

$R_Z$, $C_Z$, and $C_P$ are calculated using Equation 25, Equation 26, and Equation 27:

$$Rz = \frac{2 \times \pi \times 25000 \times 3.3 \times 54 \times 10^{-6} \times 8 \times 10^{6}}{12 \times 800 \times 0.8} = 29.2\ k\Omega \quad (28)$$

$$Cz = \frac{1}{2 \times \pi \times 6010 \times 29200} = 928\ pF \quad (29)$$

$$Cp = \frac{1}{2 \times \pi \times 103900 \times 29200} = 51\ pF \quad (30)$$

Using standard values for R3, C6, and C7 in the application schematic of Figure 13:

R3 = 29.4 kΩ

C6 = 1000 pF

C7 = 47 pF

## BOOTSTRAP CAPACITOR

Every TPS54331 design requires a bootstrap capacitor, C4. The bootstrap capacitor must be 0.1 µF. The bootstrap capacitor is located between the PH pins and BOOT pin. The bootstrap capacitor should be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

## CATCH DIODE

The TPS54331 is designed to operate using an external catch diode between PH and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the PH pin, which is VINMAX + 0.5 V. Peak current must be greater than IOUTMAX plus on half the peak to peak inductor current. Forward voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses. For this design, a Diodes, Inc. B340A is chosen, with a reverse voltage of 40 V, forward current of 3 A, and a forward voltage drop of 0.5 V.

## OUTPUT VOLTAGE LIMITATIONS

Due to the internal design of the TPS54331, there are both upper and lower output voltage limits for any given input voltage. The upper limit of the output voltage set point is constrained by the maximum duty cycle of 91% and is given by Equation 31:

$$V_{Omax} = 0.91 \times \left(\left(V_{IN\,min} - I_{O\,max} \times R_{DSon\,max}\right) + V_D\right) - \left(I_{O\,max} \times R_L\right) - V_D \quad (31)$$

Where:

$V_{IN\ min}$ = Minimum input voltage
$I_{O\ max}$ = Maximum load current
$V_D$ = Catch diode forward voltage
$R_L$ = Output inductor series resistance

The equation assumes maximum on resistance for the internal high-side FET.

The lower limit is constrained by the minimum controllable on time which may be as high as 130 ns. The approximate minimum output voltage for a given input voltage and minimum load current is given by Equation 32:

$$V_{Omin} = 0.089 \times \left(\left(V_{IN\,max} - I_{Omin} \times Rin\right) + V_D\right) - \left(I_{O\,min} \times R_L\right) - V_D \quad (32)$$

Where:

$V_{IN\ max}$ = Maximum input voltage
$I_{O\ min}$ = Minimum load current
$V_D$ = Catch diode forward voltage
$R_L$ = Output inductor series resistance

This equation assumes nominal on-resistance for the high-side FET and accounts for worst case variation of operating frequency set point. Any design operating near the operational limits of the device should be carefully checked to assure proper functionality.

## POWER DISSIPATION ESTIMATE

The following formulas show how to estimate the device power dissipation under continuous conduction mode operations. They should not be used if the device is working in the discontinuous conduction mode (DCM) or pulse skipping Eco-mode™.

The device power dissipation includes:

1) Conduction loss: Pcon = $IOUT^2$ x Rds(on) x VOUT/VIN

2) Switching loss: Psw = 0.5 x $10^{-9}$ x $VIN^2$ x IOUT x Fsw

3) Gate charge loss: Pgc = 22.8 x $10^{-9}$ x Fsw

4) Quiescent current loss: Pq = 0.11 x $10^{-3}$ x VIN

Where:

IOUT is the output current (A).

Rds(on) is the on-resistance of the high-side MOSFET (Ω).

VOUT is the output voltage (V).

VIN is the input voltage (V).

Fsw is the switching frequency (Hz).

So

Ptot = Pcon + Psw + Pgc + Pq

For given $T_A$ , $T_J = T_A$ + Rth x Ptot.

For given $T_{JMAX}$ = 150°C, $T_{AMAX} = T_{JMAX}$– Rth x Ptot.

Where:

Ptot is the total device power dissipation (W).

$T_A$ is the ambient temperature (°C).

$T_J$ is the junction temperature (°C) .

Rth is the thermal resistance of the package (°C/W).

$T_{JMAX}$ is maximum junction temperature (°C).

$T_{AMAX}$ is maximum ambient temperature (°C).

## PCB LAYOUT

The VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. The typical recommended bypass capacitance is 10-µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the source of the anode of the catch diode. See Figure 14 for a PCB layout example. The GND D pin should be tied to the PCB ground plane at the pin of the IC. The source of the low-side MOSFET should be connected directly to the top side PCB ground area used to tie together the ground sides of the input and output capacitors as well as the anode of the catch diode. The PH pin should be routed to the cathode of the catch diode and to the output inductor. Since the PH connection is the switching node, the catch diode and output inductor should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. The TPS54331 uses a fused lead frame so that the GND pin acts as a conductive path for heat dissipation from the die. Many applications have larger areas of internal or back side ground plane available, and the top side ground area can be connected to these areas using multiple vias under or adjacent to the device to help dissipate heat. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate layout schemes, however this layout has been shown to produce good results and is intended as a guideline.

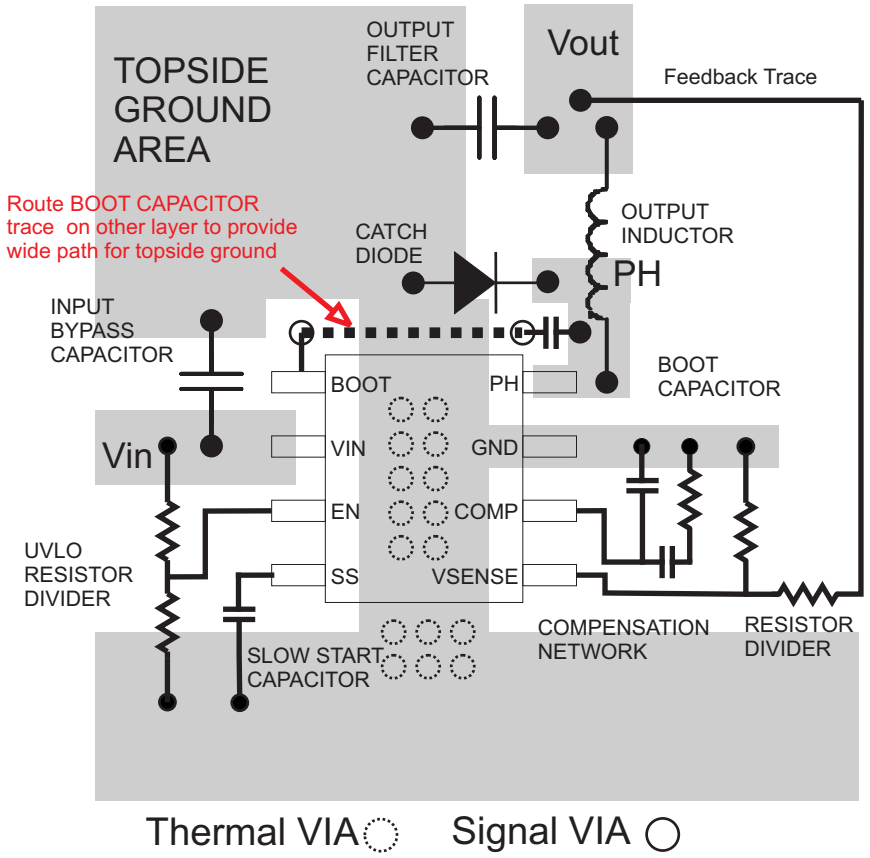



**Figure 14. TPS54331 Board Layout**

## ELECTROMAGNETIC INTERFERENCE (EMI) CONSIDERATIONS

As EMI becomes a rising concern in more and more applications, the internal design of the TPS54331 takes measures to reduce the EMI. The high-side MOSFET gate drive is designed to reduce the PH pin voltage ringing. The internal IC rails are isolated to decrease the noise sensitivity. A package bond wire scheme is used to lower the parasitics effects.

To achieve the best EMI performance, external component selection and board layout are equally important. Follow the *Step by Step Design Procedure* above to prevent potential EMI issues.

## APPLICATION CURVES

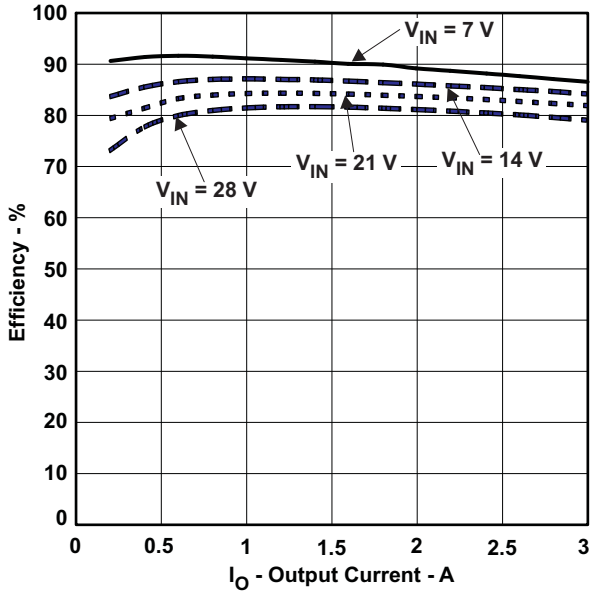



Figure 15. TPS54331 Efficiency

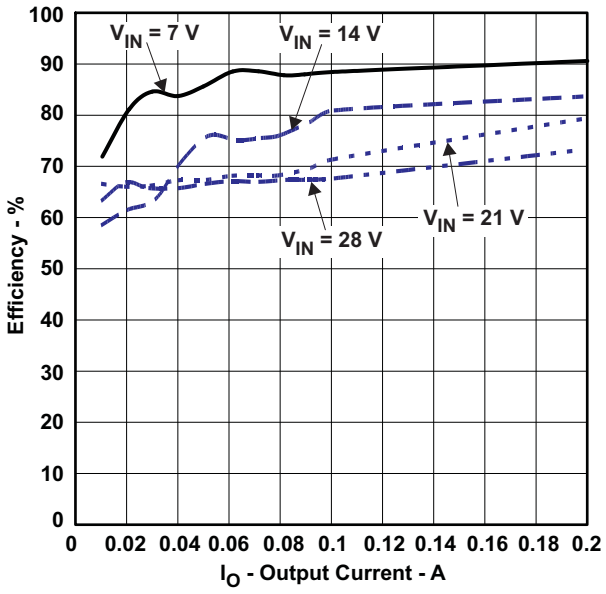



Figure 16. TPS54331 Low Current Efficiency

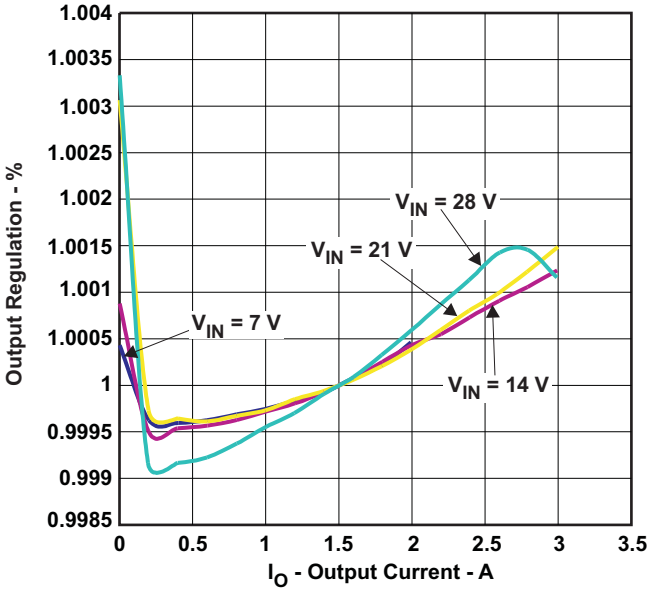



Figure 17. TPS54331 Load Regulation

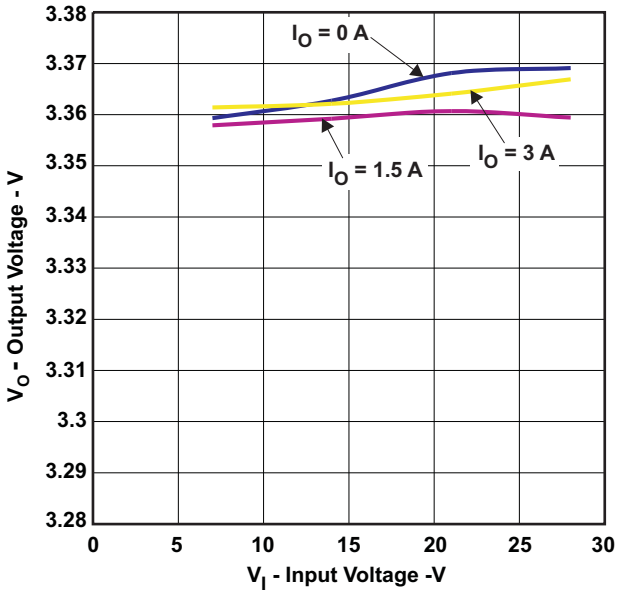



Figure 18. TPS54331 Line Regulation

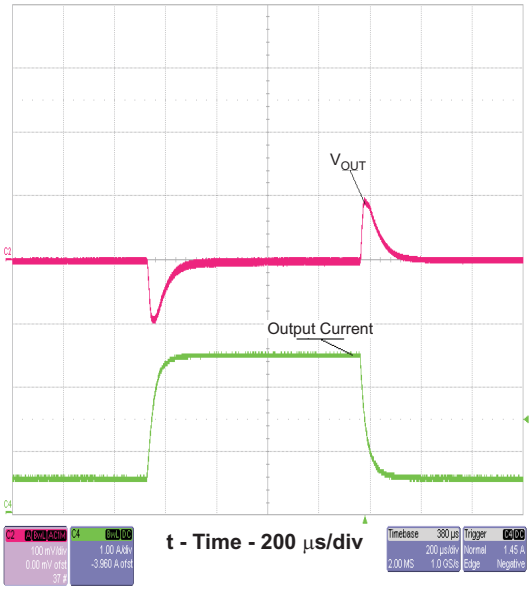



Figure 19. TPS54331 Transient Response

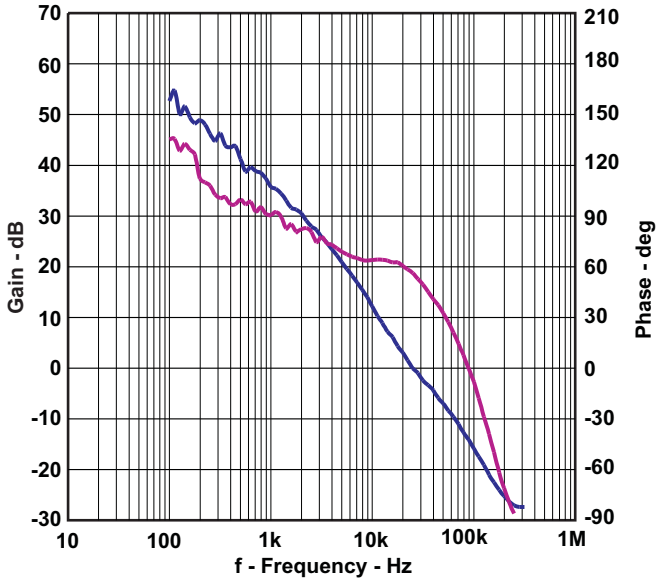



Figure 20. TPS54331 Loop Response

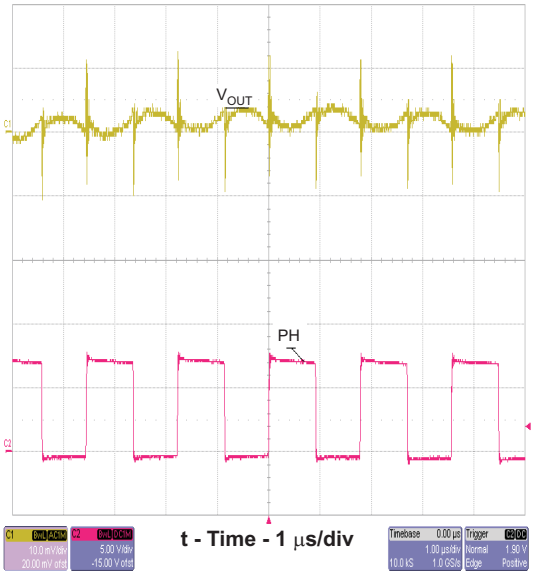



Figure 21. TPS54331 Output Ripple

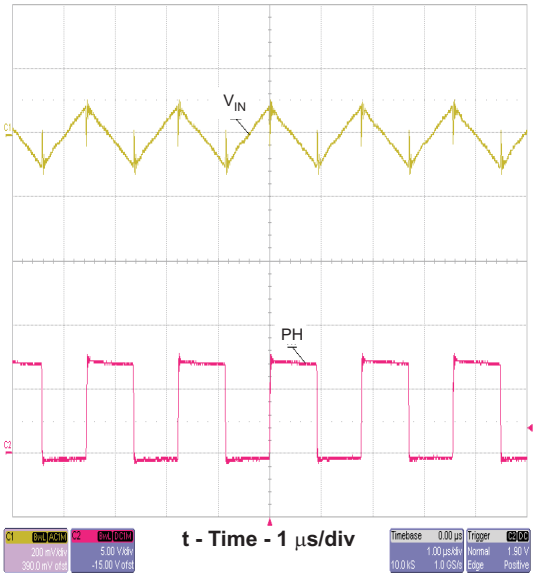



Figure 22. TPS54331 Input Ripple

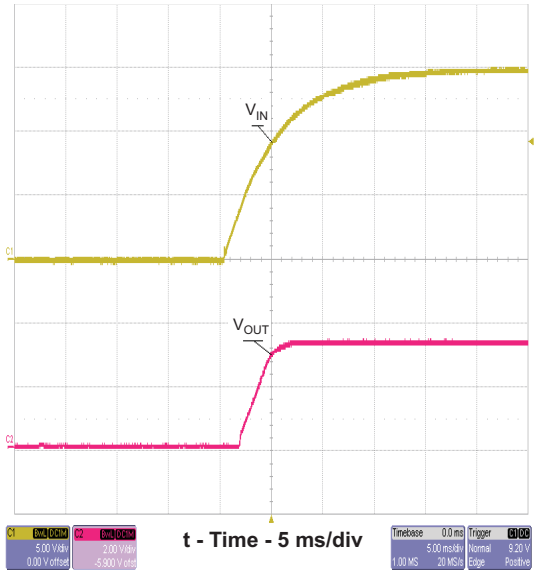



Figure 23. TPS54331 Start Up

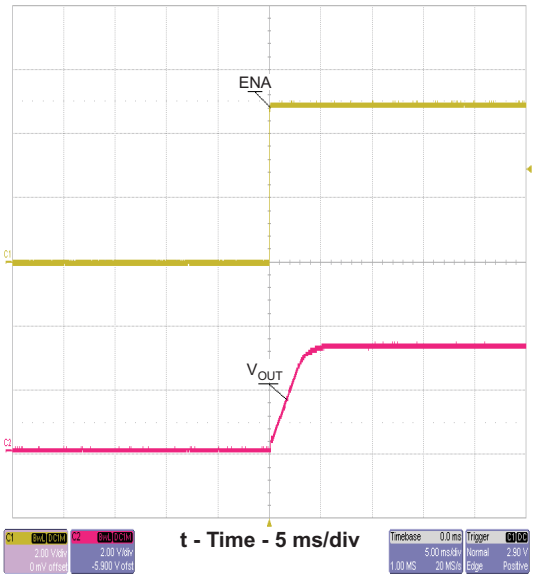



Figure 24. TPS54331 Start-up Relative to Enable

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| TPS54331D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS54331DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS54331DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS54331DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

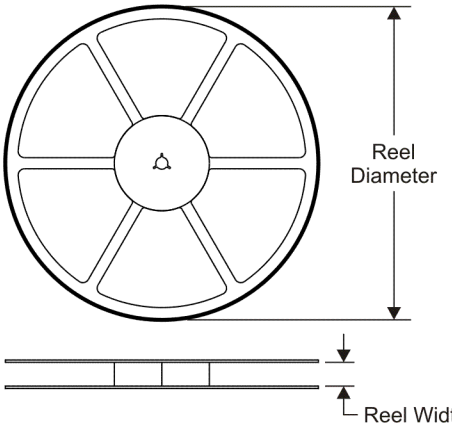
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

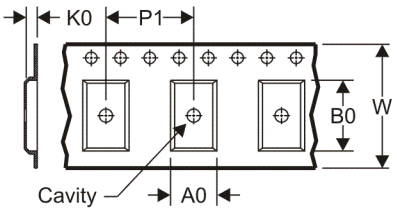
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

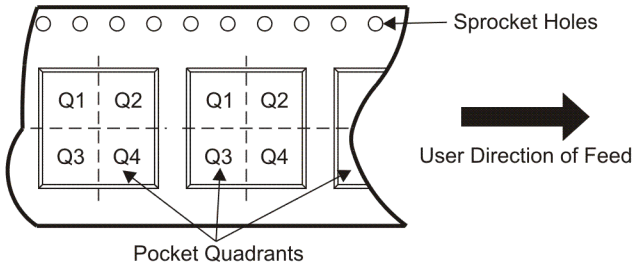



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

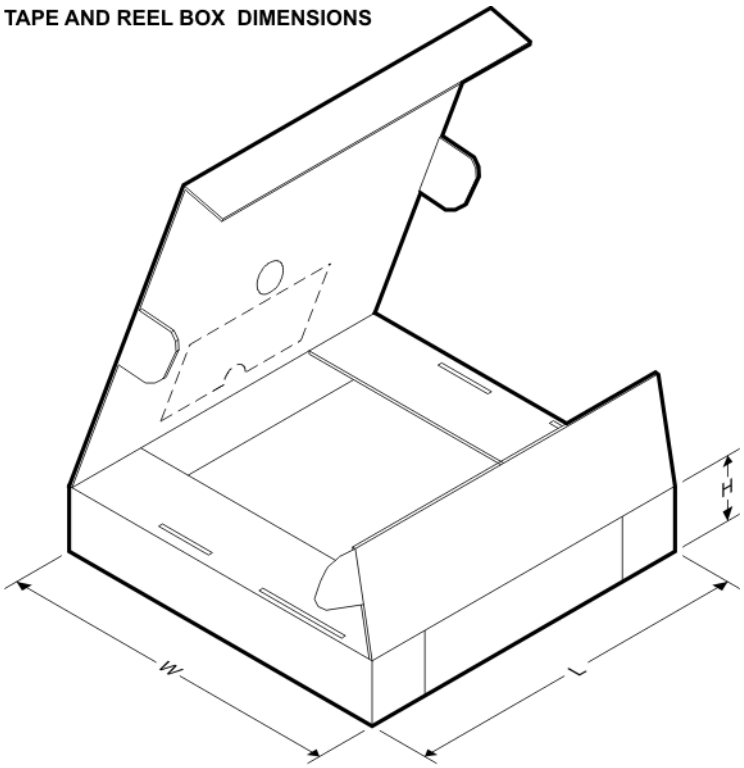
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS54331DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

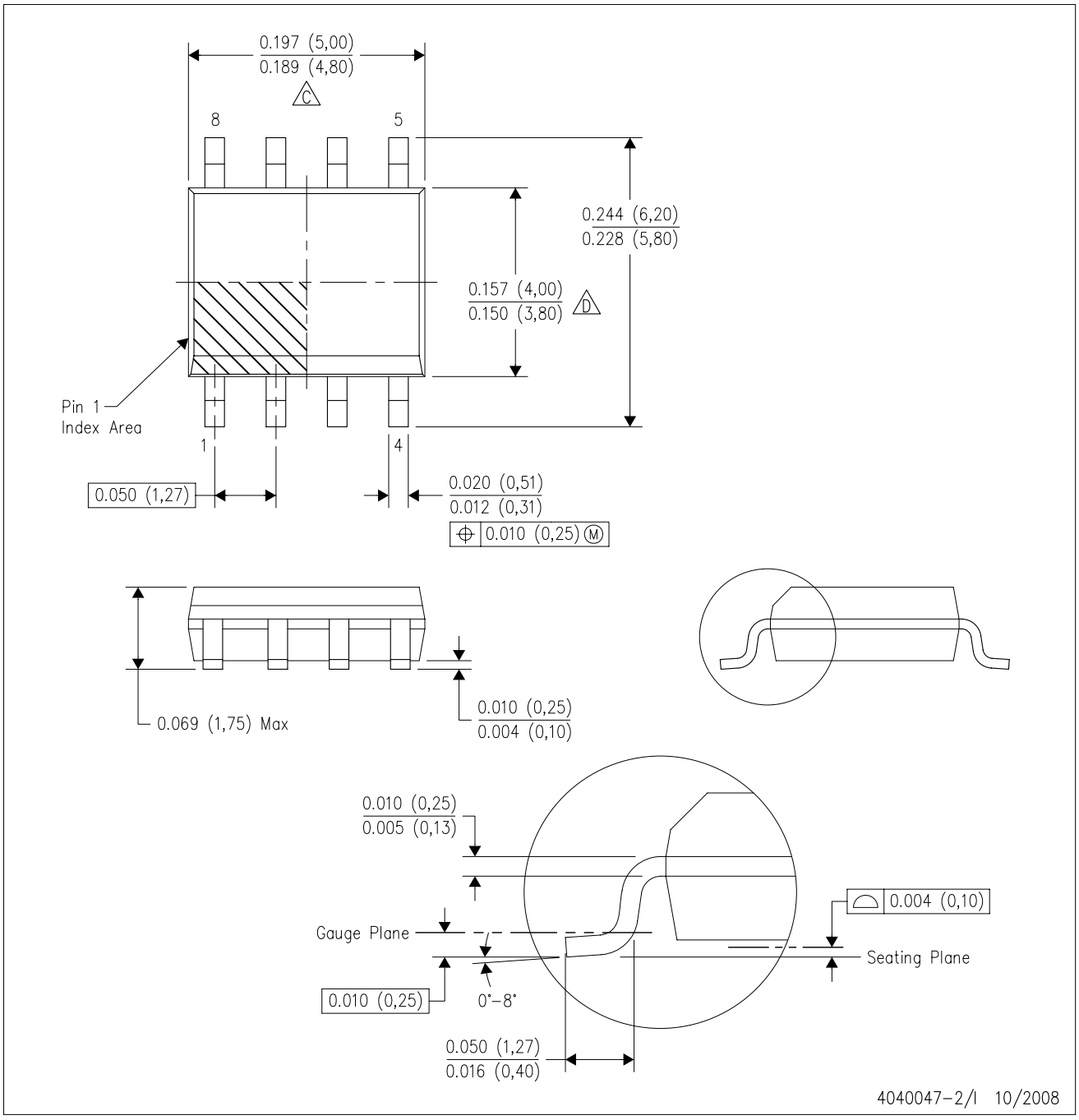
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS54331DR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Clocks and Timers | www.ti.com/clocks | Digital Control | www.ti.com/digitalcontrol |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| RFID | www.ti-rfid.com | Telephony | www.ti.com/telephony |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265